Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: G = .050” X .052”**

**Backside Potential: DRAIN**

**Mask Ref: IXB9**

**APPROVED BY: DK DIE SIZE .355” X .550” DATE: 7/21/21**

**MFG: IXYS THICKNESS .008” P/N: IXTD32P60P-B9**

**DG 10.1.2**

#### Rev B, 7/19/02